**What is claimed is:**

1. A circuit comprising:

a plurality of logic elements to receive at least one bit of a first input mantissa and at least one bit of a second input mantissa;

said plurality of logic elements to generate and transmit a predictive bit stream including an indicating bit in one of a bit position before a leading zero and before a leading one of the sum of said mantissas;

a counter to generate a predictive count equal to a number of bits between a first bit generated of the predictive bit stream and said indicating bit in the predictive bit stream, wherein said counter is to transmit a predictive count.

2. The circuit of claim 1 wherein said plurality of logic elements is an LZA device.

3. A circuit comprising:

a plurality of logic elements to receive at least one bit of a first input mantissa and at least one bit of a second input mantissa;

said plurality of logic elements to generate and transmit a predictive bit stream including an indicating bit in one of a bit position before a leading zero and a leading one of the sum of said mantissas;

a counter to generate and transmit a predictive count equal to a number of bits between a first bit generated of the predictive bit stream and said indicating one bit in the predictive bit stream;

an adder circuit to receive said input mantissas and calculate a sum of said input

mantissas;

a shifter circuit to receive said sum from the adder circuit and said predictive count from the plurality of logic elements, and to shift said sum to remove leading zeroes positioned in more significant positions than a most significant bit of the sum, wherein said shifting is performed a number of times equal to said predictive count;

a compensatory shifter circuit to receive the shifted sum and to shift the sum to the left by zero to two bits to remove any remaining leading zeros.

4. The circuit of claim 3, wherein the plurality of logic elements each are to accept consecutive bits of the first and second input mantissas in groups of three and each group includes at least two bits from a previous group.

5. The circuit of claim 4, wherein the plurality of logic elements is to receive a plurality of groups of three bits from a first input mantissa and a plurality of groups of three bits from a second input mantissa, wherein the first groups of bits received are the most significant bits in the input mantissas, and subsequent groups are received whose bits are less significant than the bits of the previously received bit groups by one bit position.

6. The circuit of claim 5, wherein a number of bits entering the plurality of logic elements is exactly three for each mantissa.

7. The circuit of claim 6, wherein the plurality of logic elements is to generate a one if the addition of the three bits of the first and second input mantissas with a carry bit will produce a three bit sum in which the first two bits are one of 0 and 1 respectively and 1 and 0 respectively for at least one value of the carry bit.

8. The circuit of claim 7, wherein the generated bits make up the predictive bit stream.

9. The circuit of claim 3, wherein the plurality of logic elements each are to simultaneously accept bits of the first and second input mantissas in groups of three and each group includes at least two bits from a previous group.

10. The circuit of claim 9, wherein the plurality of logic elements receive a plurality of groups of three bits from a first input mantissa and a plurality of groups of three bits from a second input mantissa, the first groups of bits received are the most significant bits in the input mantissas, subsequent groups are received whose bits are less significant than the bits of the previously received bit groups by one bit position.

11. The circuit of claim 10, wherein the adder circuit is to transmits a sum and a two's complement of the sum of the input mantissas.

12. The circuit of claim 11, wherein the input mantissas are carry and sum parts of an addition result and the addition is performed in a redundant carry-save format.

13. A method of anticipating one of a number of leading zero and leading one bits in a sum of two numbers, the method comprising:

receiving by a plurality of logic elements a plurality of groups of three bits from a first input mantissa and a plurality of groups of three bits from a second input mantissa, wherein the first groups of bits received are the most significant bits in the input mantissas, subsequent groups are received whose bits are less significant than the bits of the previously received bit groups by one bit position;

generating a predictive bit stream by the plurality of logic elements possessing an indicating bit in a bit position before one of a leading zero and a leading one of the sum of said mantissas, wherein the predictive bit stream has a one in a bit position if the addition of the corresponding group of three bits from first input mantissa and the corresponding group of three bits from second input mantissa with a carry bit produces a three bit sum in which a first two bits of the sum are one of 0 and 1 respectively and 1 and 0 respectively for at least one value of the carry bit, and otherwise has a zero in that bit position;

transmitting the predictive bit stream to a counter; and

generating a predictive count by a counter equal to a number of bits between a first bit generated by the predictive bit stream and said indicating bit in the predictive bit stream.

14. The method of claim 13 comprising receiving said input mantissas and calculating a sum of said input mantissas and transmitting a bit stream representing the sum of the mantissas.

15. The method of claim 14 further comprising receiving said sum from the adder circuit and said predictive count from the plurality of logic elements, shifting said sum to remove leading zeroes positioned in more significant positions than a most significant bit of the sum, wherein said shifting is performed a number of times equal to said predictive count.

16. The method of claim 15 further comprising receiving the shifted sum and shifting the sum to the left by zero to two bits to remove remaining leading zeroes.

17. The method of claim 16, wherein the bits enter the plurality of logic elements in groups of three for each mantissa.

18. The method of claim 17, wherein the adder generates a sum and 2's complement of the sum of the input mantissas and transmits the positive result as the sum.